HARRIS Semiconductor

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CD22402

Sync Generator for TV Applications and Video Processing Systems

May 1999

Features

- **Interlaced Composite Sync Output**
- **Automatic Genlock Capability**
- **Crystal Oscillator Operation**
- **525 or 625 Line Operation**
- **Vertical Reset Option**
- **Wide Power Supply Operating Voltage . . . . . 4V to 15V**

Applications

- **Cameras**
- **Monitors and Displays**
- **CATV**
- **Teletext**
- **Video Games**
- **Sync Restorer**
- **Video Service Instruments**

Part Number Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CD22402D	-55 to 125	24 Ld SBDIP	D24.6
CD22402E	-40 to 85	24 Ld PDIP	E24.6

Description

The Harris CD22402 (Note) is a CMOS LSI sync generator that produces all the timing signals required to drive a fully 2-to-1 interlaced 525-line 30-frame/second, or 625-line 25-frame/second TV camera or video processing system. A complete sync waveform is produced which begins each field with six serrated vertical sync pulses, preceded and followed by six half-width double frequency equalizing pulses. The sync output is gated by the master clock to preserve horizontal phase continuity during the vertical interval.

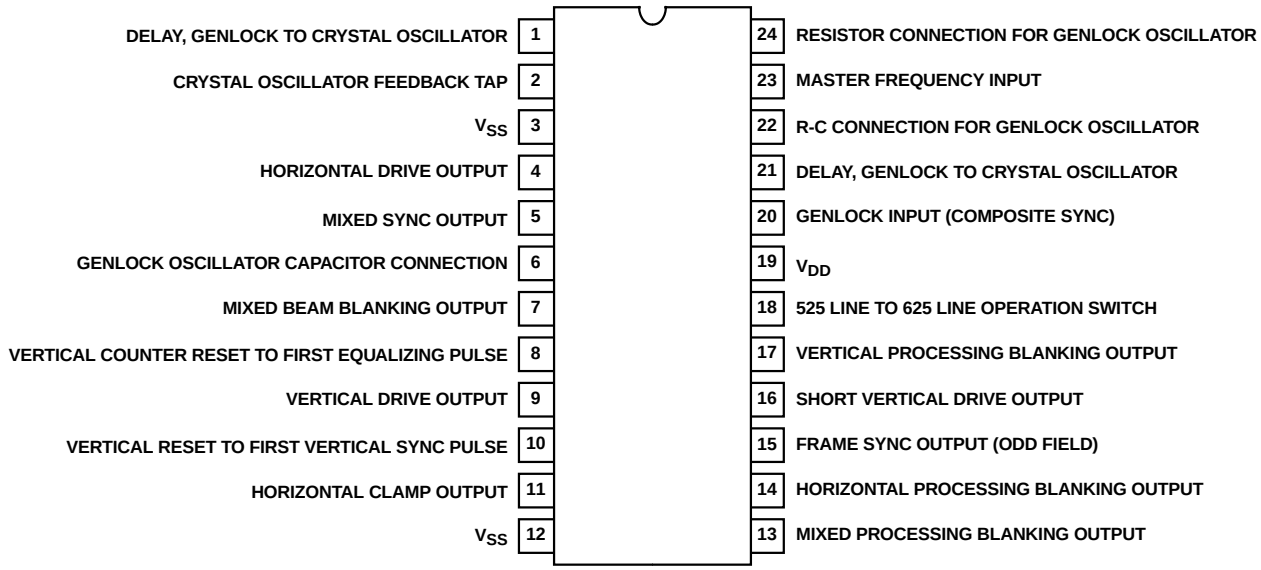
The CD22402 can be operated either in “genlock” mode, in which it is synchronized with a reference sync pulse train from another TV camera, or in “stand-alone” mode, in which it is synchronized with a local on-chip crystal oscillator (the crystal and two passive components are off chip). Also, the circuit can sense the presence or absence of a reference sync pulse train and automatically select the “genlock” or “stand-alone” mode.

A frame sync pulse is produced at the beginning of every odd field. The vertical counter can be reset to either the first equalizing pulse or the first vertical sync pulse of the vertical interval. The interlaced sync provided by the CD22402 differs from RS-170 by having slightly narrower sync and equalizing pulses. The clock frequency of 32 times horizontal rate allows for approximately 4μs horizontal pulse widths and 2μs equalizing pulses. Otherwise operation can be phase locked to a color sub-carrier for a full interlaced operating system.

The CD22402 is operable with a single supply over a voltage range of 4V to 15V.

Pinout

CD22402 (PDIP, SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1686.5**

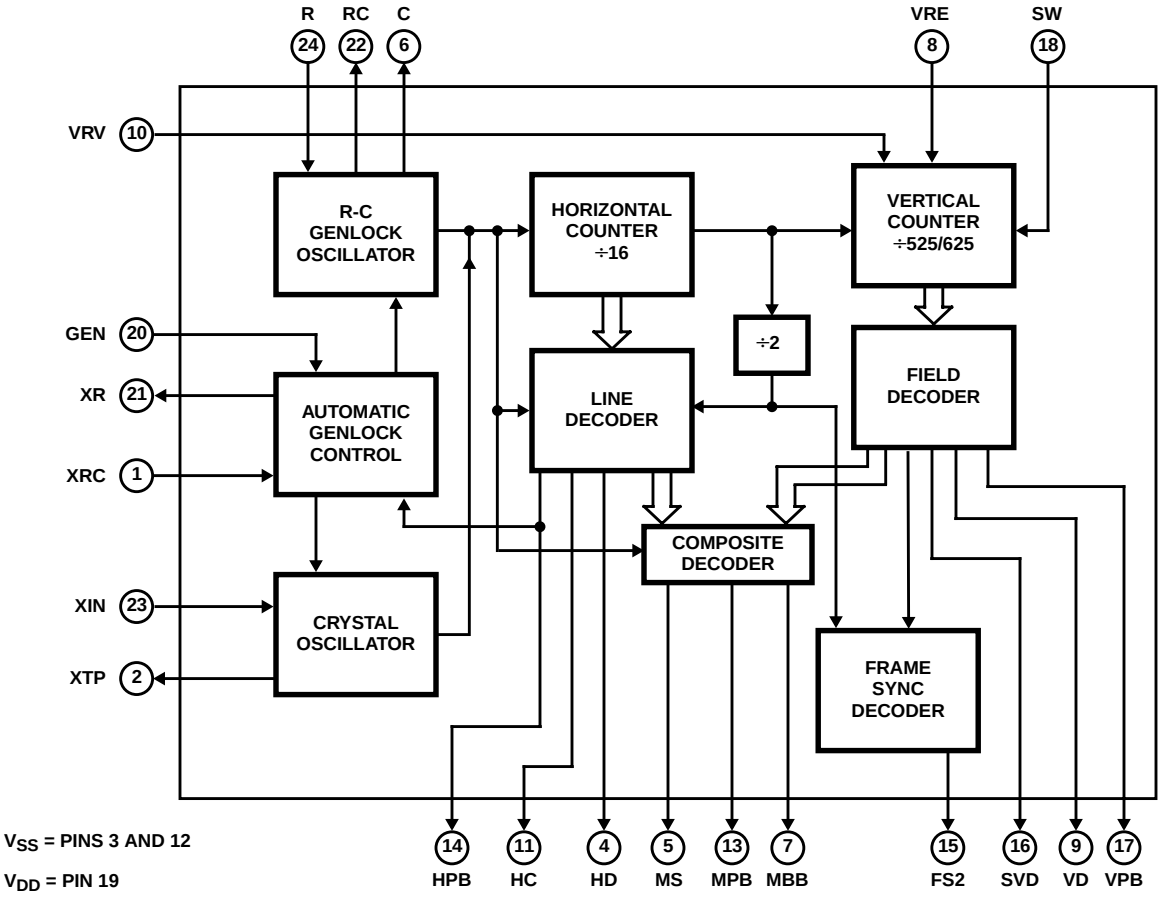
Pin Descriptions

PIN NO.	SYMBOL	DESCRIPTION
1	XRC	**Delay, Genlock to Crystal Oscillator.** Resistor, diode and capacitor connection for delay that automatically turns on the crystal oscillator when the genlock input is removed. When the signal on Terminal 1 is high the crystal oscillator is inhibited. Typical values for R and C are 1MΩ and 0.001µF. For operation as a crystal controlled stand alone sync generator without genlock, Terminal 1 should be hardwired to V_{SS}.
2	XTP	**Crystal Oscillator Feedback Tap.** Feedback connection (tap) for crystal oscillator. When a crystal (shunted by a 1MΩ resistor) is connected between this terminal and Terminal 23, and a 100pF capacitor is connected from this terminal to V_{SS}, the sync generator creates its own master frequency. For a 525-line, 30-frame/second raster, the crystal frequency is 504.000kHz (Note 1); and for a 625-line, 25-frame/second raster, the crystal frequency is 500.000kHz (Note 1).
3	V_{SS}	**Negative Power Supply Voltage.** This terminal must be hardwired to Terminal 12 (V_{SS}).
4	HD	**Horizontal Drive Output**
5	MS	**Mixed Sync Output**
6	C	**Capacitor Connection for R-C Genlock Oscillator**
7	MBB	**Mixed Beam Blanking Output**
8	VRE	**Vertical Counter Reset to First Equalizing Pulse.** A low level signal on this terminal resets the vertical counter to the first equalizing pulse of a field. When not in use this terminal should be connected to V_{DD}.
9	VD	**Vertical Drive Output**
10	VRV	**Vertical Counter Reset to First Vertical Sync Pulse.** A low level signal on this terminal resets the sync generator to the first vertical sync pulse of a field. For genlock operation, Terminal 10 is used as a resistor and capacitor connection for an integrator network that detects vertical sync pulses in a master sync waveform to which the sync generator is to be genlocked. R is 22kΩ, and C is 0.001µF. When not in use this terminal should be connected to V_{DD}.
11	HC	**Horizontal Clamp Output**
12	V_{SS}	**Negative Power Supply Voltage**
13	MPB	**Mixed Processing Blanking Output**
14	HPB	**Horizontal Processing Blanking Output**
15	FS2	**Frame Sync Output (Odd Field).** A pulse coinciding with the first equalizing pulse is produced at the beginning of every odd field.
16	SVD	**Short Vertical Drive Output**
17	VPB	**Vertical Processing Blanking Output**
18	SW	**Operation Switch for 525-Line or 625-Line Raster.** A high level signal on Terminal 18 causes the sync generator to generate a 625-line raster. An internal pulldown resistor is connected to Terminal 18, so in the absence of an applied input to this terminal, a 525-line raster is produced.
19	V_{DD}	**Positive Power Supply Voltage.** V_{DD} can be any voltage between +4 and +15 relative to V_{SS}.
20	GEN	**Genlock Input Composite Sync.** A negative going reference mixed sync waveform applied to Terminal 20 disables the crystal oscillator and locks the R-C genlock oscillator to the horizontal pulses of the reference sync waveform. Vertical sync detection is achieved by an R-C integrator connected from Terminal 20 to Terminal 10 (vertical reset to first vertical sync pulse). An internal pull-up resistor is connected to Terminal 20 so that in the absence of an applied input the crystal oscillator is enabled and the R-C genlock oscillator is disabled.
21	XR	**Delay, Genlock to Crystal Oscillator, Resistor and Diode Connection for Delay, Genlock to Crystal Oscillator.** Automatically turns on the crystal oscillator when the input to Terminal 20 is removed.
22	RC	**Resistor and Capacitor Connection for Genlock Oscillator.** If the genlock oscillator is not used this terminal should be connected to V_{SS}. C should be 100pF, and R should be a 10kΩ potentiometer.
23	XIN	**Master Frequency Input.**
24	R	**Resistor Connection for Genlock Oscillator.**

NOTE: 32 times horizontal frequency.

Block Diagram

CD22402 MONOCHROME TV SYNC GENERATOR WITH AUTOMATIC GENLOCK



Absolute Maximum Ratings

DC Supply Voltage (Referenced to V_{SS} Terminal) 15V
Input Voltage Range, All Inputs (Notes 2, 3) . . . . . $V_{SS} \le V_I \le V_{DD}$
DC Input Current, Any One Input (Note 2) . . . . . ±10mA

Operating Conditions

Temperature Range
CD22402D . . . . . -55^oC to 125^oC
CD22402E . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	50	10
PDIP Package	50	N/A

Maximum Junction Temperature (SBDIP Package) . . . . . 175^oC
Maximum Junction Temperature (PDIP Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10mA even when the power is off.
3. A connection must be provided at every input terminal. All unused inputs must be connected to V_{DD} or V_{SS}, whichever is appropriate.

Electrical Specifications

Values at -55^oC, 25^oC, 125^oC Apply to D Package
Values at -40^oC, 25^oC, 85^oC Apply to E Package

PARAMETER	SYMBOL	TEST CONDITIONS									
		V_O (V)	V_{DD} (V)	-55^oC	-40^oC	85^oC	125^oC	25^oC MIN	25^oC TYP	25^oC MAX	UNITS
DC ELECTRICAL SPECIFICATIONS											
Quiescent Device Current	I_{DD} (Max)	-	5	-	-	-	-	0.5	0.75	1	mA
		-	10	-	-	-	-	1.5	2	2.5	mA
		-	15	-	-	-	-	3	4	5	mA
Output Low (Sink) Current	I_{OL} (Min)	0.5	5	100	96	66	56	80	160	-	µA
		5	5	1200	1155	787	672	960	1920	-	µA
		0.5	10	248	239	164	140	200	400	-	µA
		10	10	3000	2868	1968	1680	2400	4800	-	µA
Output High (Source) Current	I_{OH} (Min)	4.5	5	-100	-96	-66	-56	-80	-160	-	µA
		0	5	-1200	-1155	-787	-672	-960	-1920	-	µA
		9.5	10	-248	-239	-164	-140	-200	-400	-	µA
		0	10	-3000	-2868	-1968	-1680	-2400	-4800	-	µA
Output Voltage Low Level	V_{OL} (Max)	-	5	0.15	0.15	0.15	0.15	-	-	0.15	V
		-	10	0.15	0.15	0.15	0.15	-	-	0.15	V
Output Voltage High Level	V_{OH} (Min)	-	5	4.85	4.85	4.85	4.85	4.85	-	-	V
		-	10	9.85	9.85	9.85	9.85	9.85	-	-	V
Input Low Voltage	V_{IL} (Max)	0.5, 4.5	5	1.5	1.5	1.4	1.4	-	2.25	1.5	V
		1, 9	10	3	3	2.9	2.9	-	4.5	3	V
Input High Voltage	V_{IH} (Min)	0.5, 4.5	5	3.6	3.6	3.5	3.5	3.5	2.25	-	V
		1, 9	10	7.1	7.1	7	7	7	4.5	-	V
Input Current	I_{IN} (Max)	-	-	-	-	-	-	-	10	-	pA

Refer to the CD4000B Series data book 250.5 for general operating and application considerations.

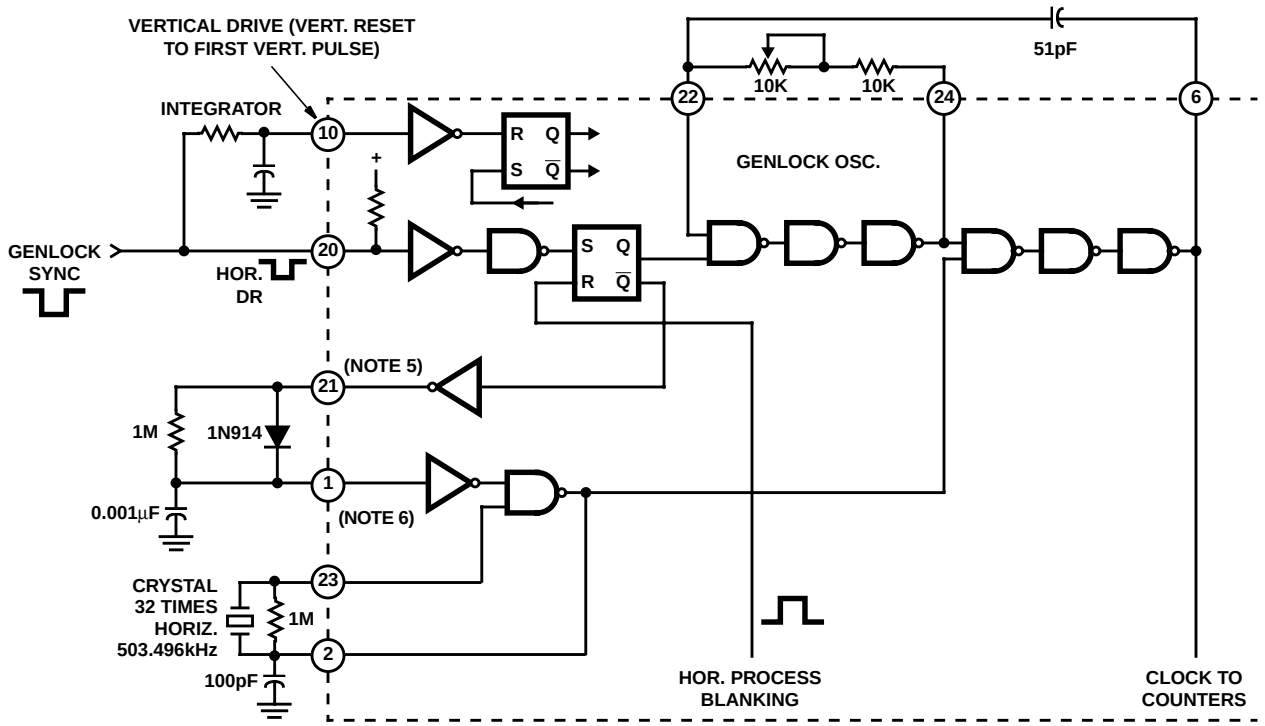
Switching Electrical Specifications $T_A = 25^oC$ and $C_L = 15pF$. Typical Temperature Coefficient for All Values of $V_{DD} = 0.3\%/^oC$

PARAMETER (NOTE 4)	SYMBOL	TEST CONDITIONS V_{DD} (V)	MIN	TYP	MAX	UNITS
Output State Propagation Delay Time (50% to 50%)						
Low-to-High Level	t_{PLH}	5	-	40	80	ns
High-to-Low Level	t_{PHL}	10	-	20	40	ns
Output State Transition Time (10% to 90%)						
Low-to-High	t_{TLH}	5	-	45	90	ns
High-to-Low	t_{THL}	10	-	30	60	ns
Input Capacitance (Per Input)	C_I	-	-	5	-	pF

NOTE:

4. The characteristics given are defined for unbuffered gate in the CMOS process of the CD22402.

Logic Diagram



NOTES:

5. Pin 21 high when pin 20 is high (or open).
6. Pin 1 high inhibits clock.

FIGURE 1. DETAIL OF THE OSCILLATOR/GENLOCK PORTION OF THE CD22402

Timing Waveforms

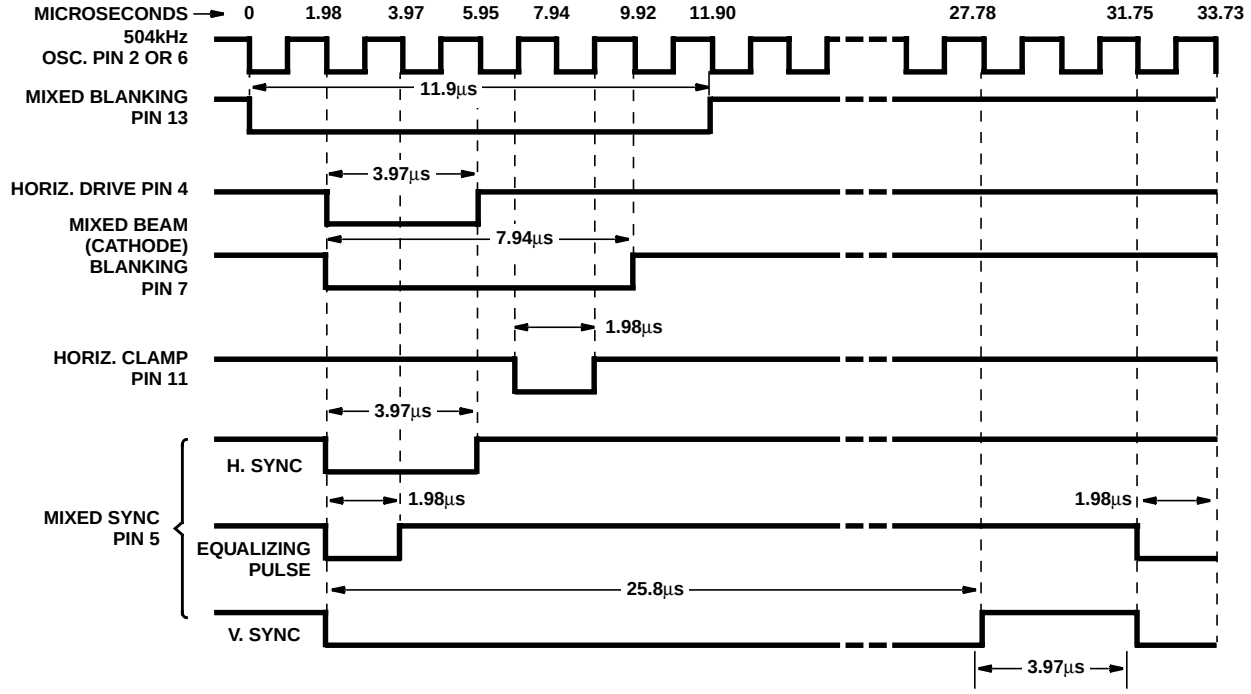


FIGURE 2. SYNC GENERATOR TIMING - 525/60Hz, HORIZONTAL TIMING WAVEFORMS

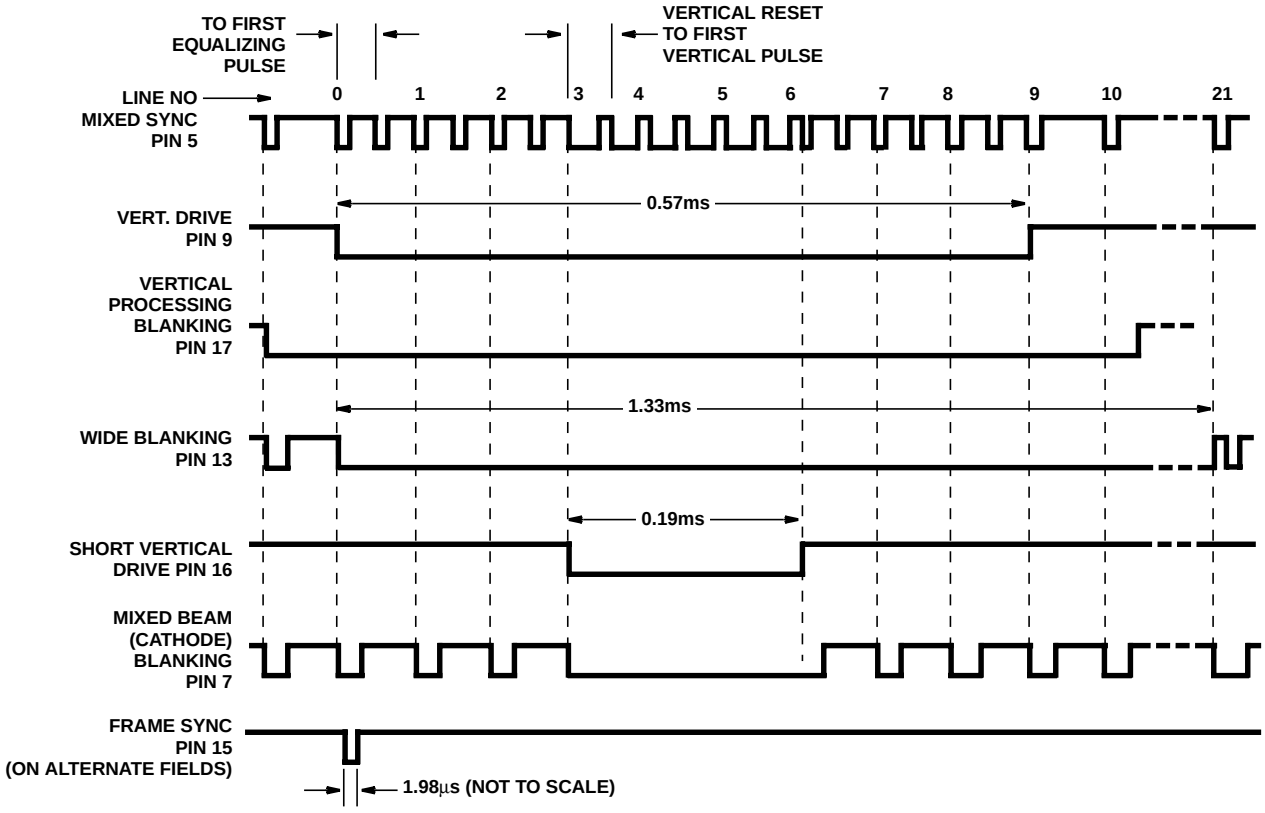


FIGURE 3. SYNC GENERATOR TIMING - 525/60Hz, VERTICAL TIMING WAVEFORMS

Timing Waveforms (Continued)

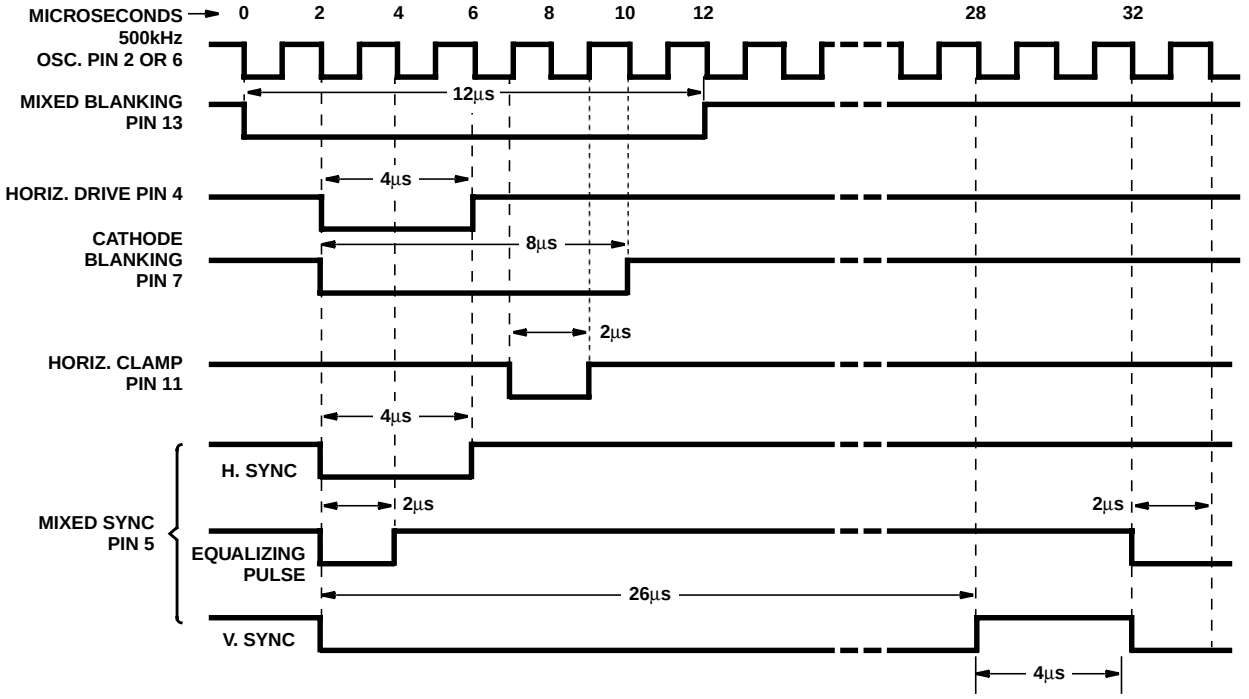


FIGURE 4. SYNC GENERATOR TIMING - 625/50Hz, HORIZONTAL TIMING WAVEFORMS

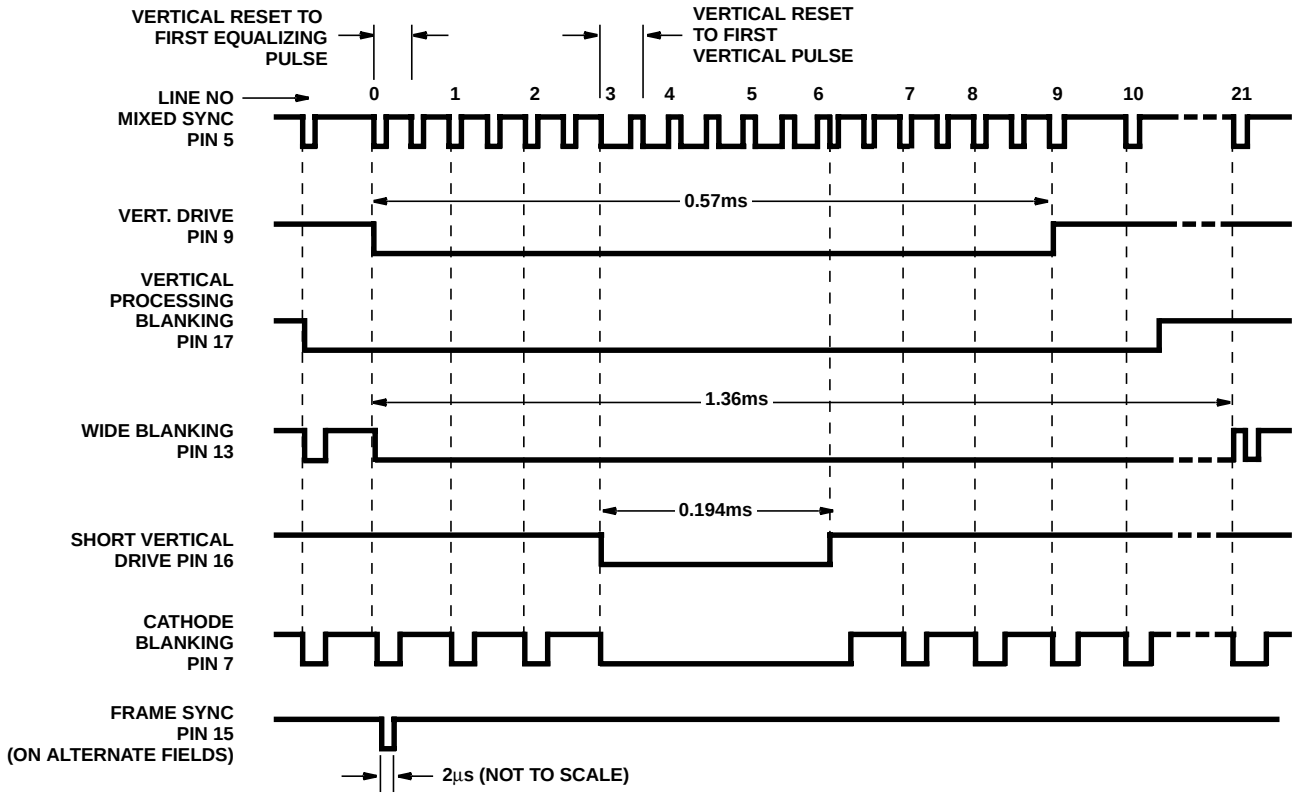


FIGURE 5. SYNC GENERATOR TIMING - 625/50Hz, VERTICAL TIMING WAVEFORMS

Timing Waveforms (Continued)

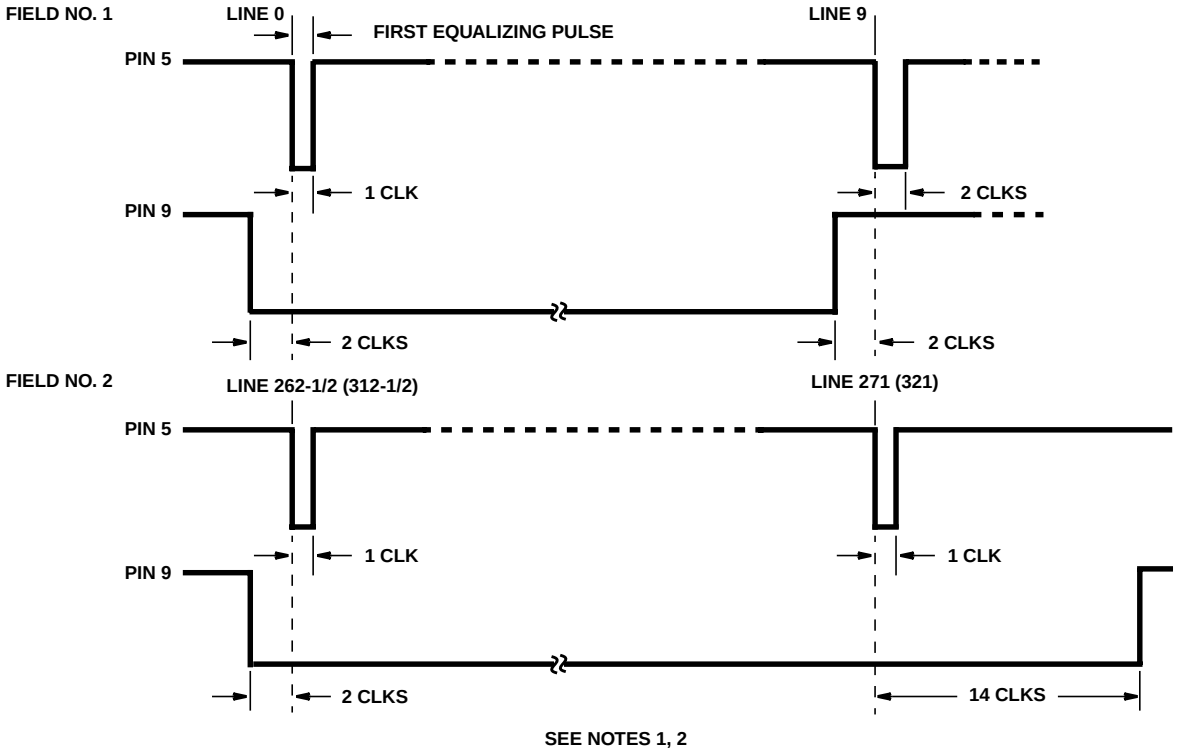


FIGURE 6. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (VERTICAL DRIVE - PIN 9)

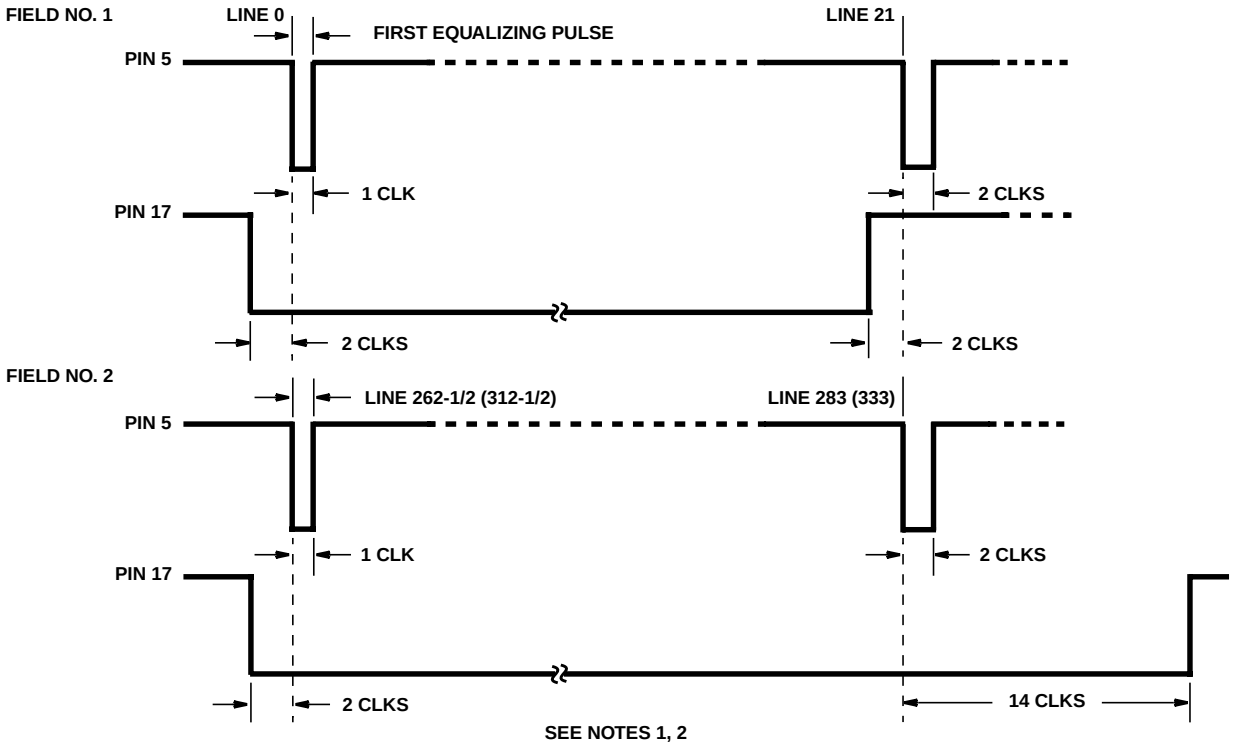


FIGURE 7. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (VERTICAL PROCESSING BLANKING - PIN 17)

Timing Waveforms (Continued)

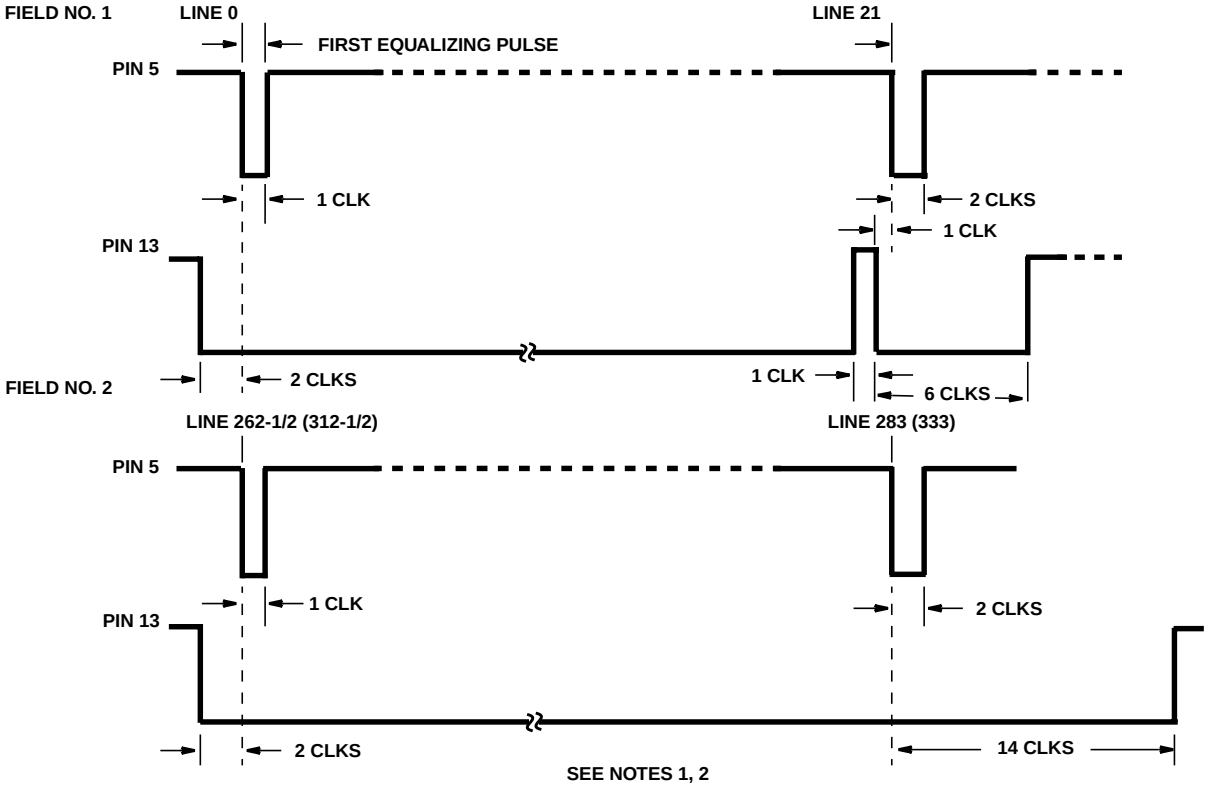


FIGURE 8. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (MIXED PROCESSING BLANKING - PIN 13)

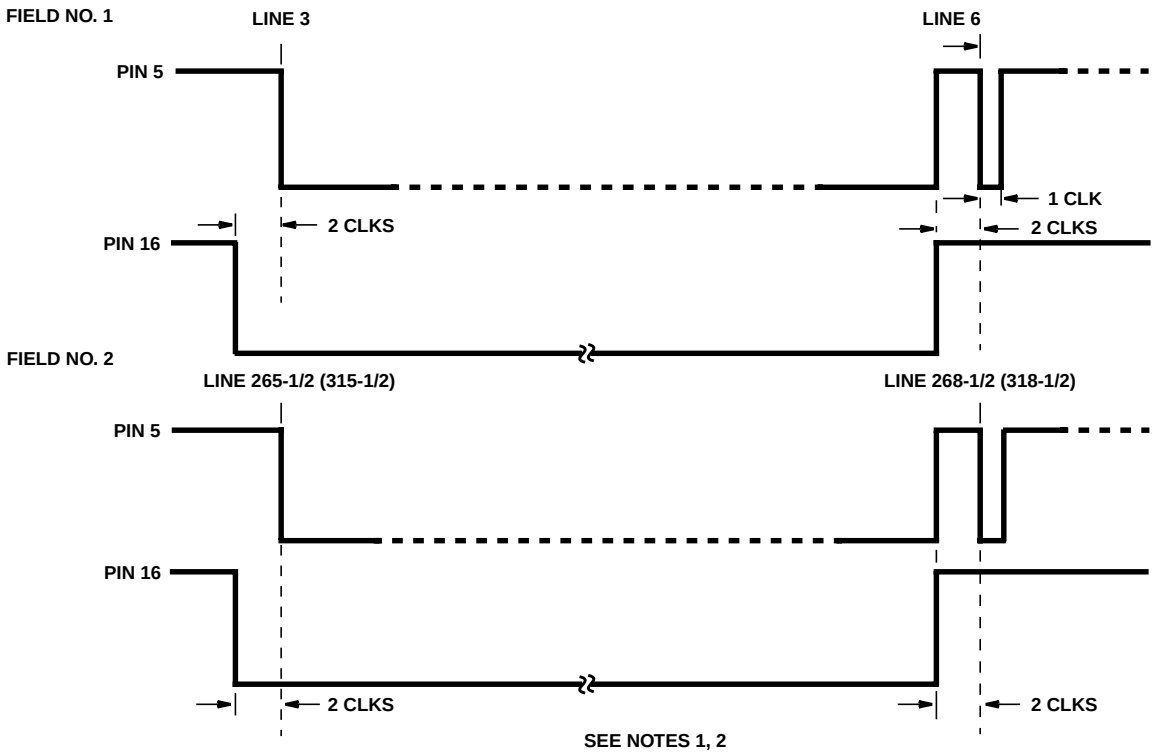
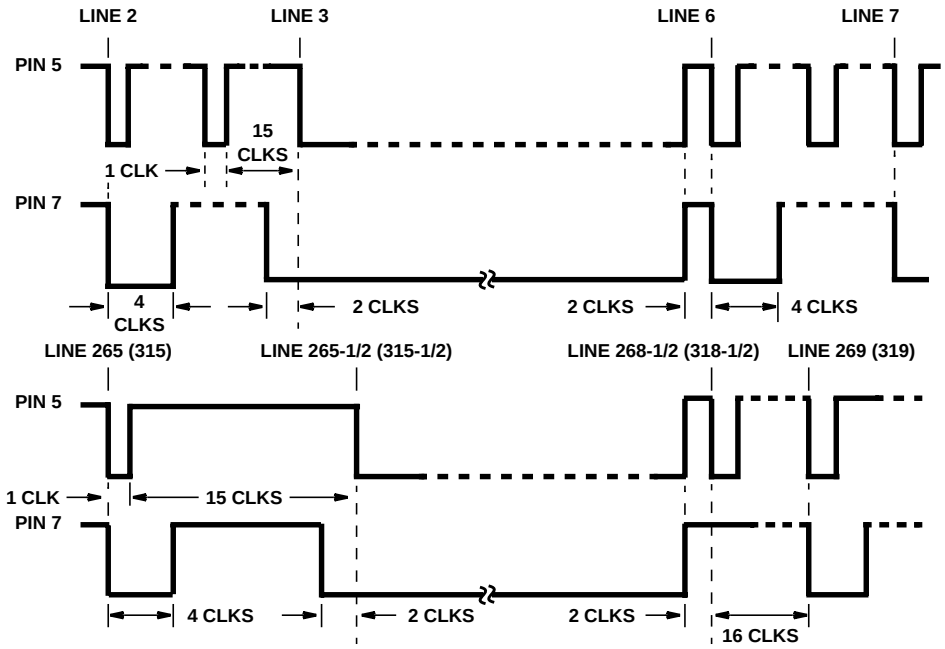


FIGURE 9. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (SHORT VERTICAL DRIVE - PIN 16)

Timing Waveforms (Continued)



NOTES:

7. Waveforms shown are for 525 line/60Hz, line number in parenthesis are for (625 line/50Hz).
8. Timing widths by clock count; for 525 line, 1 CLK = 1.98µs; for 625 line, 1 CLK = 2µs; 1 horizontal period = 32 CLKS.

FIGURE 10. EXPANDED VERTICAL-TIMING WAVEFORM DETAIL OF SYNC GENERATOR TIMING (MIXED BEAM BLANKING - PIN 7)

Typical Applications (Refer to Application Note AN8742, for more information)

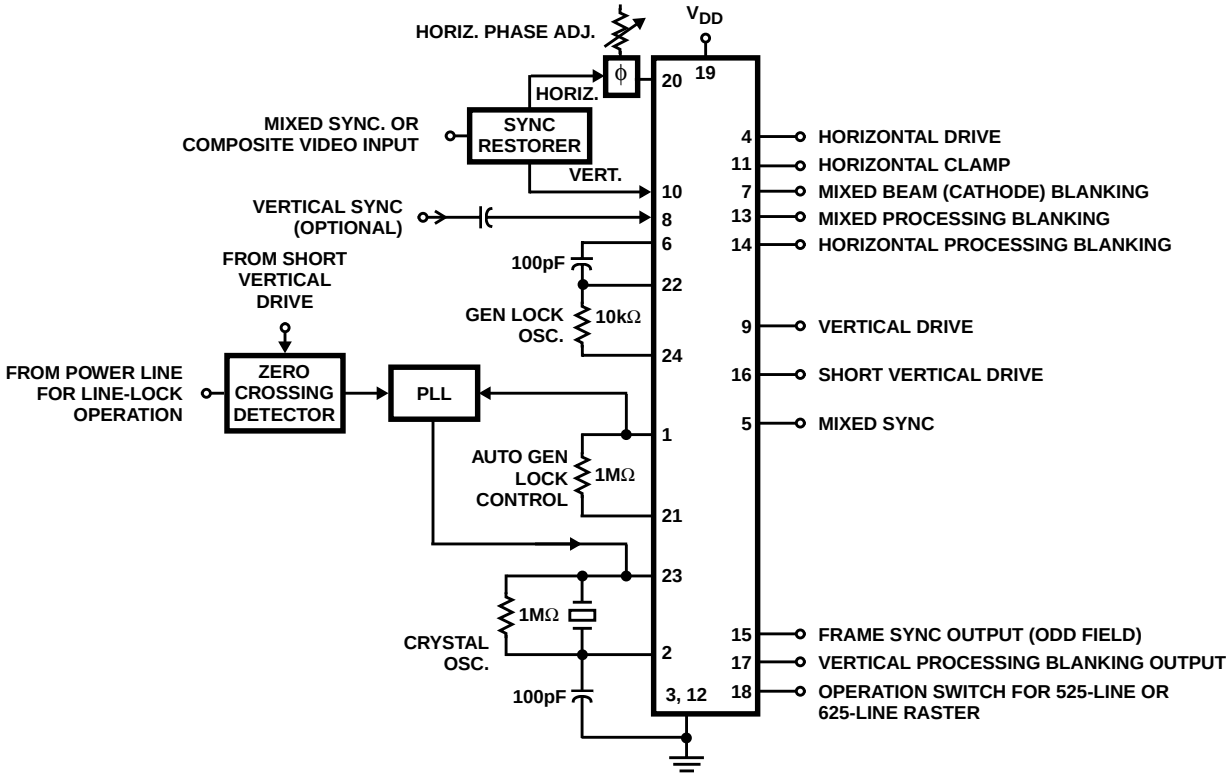
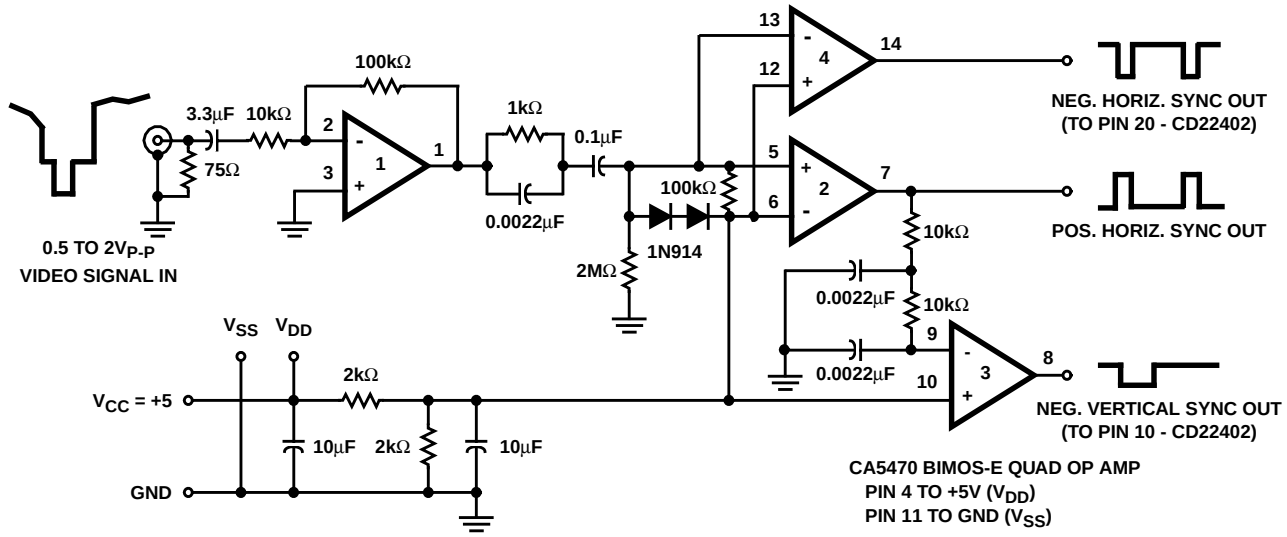


FIGURE 11. TYPICAL APPLICATION IN A TV CAMERA



NOTE: The genlock input to pins 10 and 20 of the CD22402 are direct coupled to the output from Pins 8 and 14 of the CA5470. Refer to Application Note AN-8742 for additional information.

FIGURE 12. SUGGESTED SYNC-SEPARATOR CIRCUIT USING THE CA5470 BIMOS-E QUAD OP AMP IN THE V_{DD} RANGE OF 4V TO 12V